2012 IC Design Contest at YZU

Designing an 8-bit ALU

Please complete the schematic and the physical layout of an 8-bit **78x382-like** arithmetic logic unit (ALU). Note that the inputs and outputs of the ALU are shown in Figure 1, and its logic functions are listed in Table 1. Your layout design must pass DRC, LVS, and post-layout simulations. Also, please write a report which contains the followings:

(1) Results of pre-layout simulations for verifying your schematic design. (Please describe the methods you used for verifying your schematic design.)

(2) Results of post-layout simulations for verifying the functions of your design. (Please describe the methods you used for verifying the functions of your design.)

(3) The propagation delays of your ALU (including t_{pdr} and t_{pdf}) in pre-layout and post-layout simulations. (Please describe the methods you used.)

(4) The rise times t_r in pre-layout and post-layout simulations. (Please describe the methods you used.)

(5) The fall times t_f in pre-layout and post-layout simulations. (Please describe the methods you used.)

(6) The width and the height of your complete ALU layout (in terms of microns).

(7) The screenshots of your complete schematic and your complete layout.

(8) The things that you have learned through the whole process of designing the ALU.

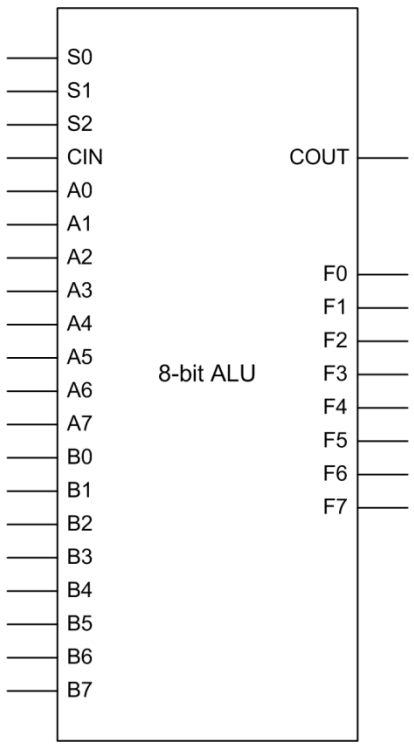

Figure 1.

Table 1.

Inputs			***Function***
S2	S1	S0	
0	0	0	F = 00000000 COUT = 0
0	0	1	F = B minus A minus 1 plus CIN COUT = F8
0	1	0	F = A minus B minus 1 plus CIN COUT = F8
0	1	1	F = A plus B plus CIN COUT = F8
1	0	0	F = A $\oplus$ B COUT = not CIN
1	0	1	F = A + B COUT = CIN
1	1	0	F = A · B COUT = CIN
1	1	1	F = 11111111 COUT = 1